

IN THE CLAIMS

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently Amended) A carry save adder circuit for reducing the number of inputs to a lower number of outputs, said carry save adder circuit comprising four carry save adders, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a second of said layers, said third and fourth carry save adders being arranged to provide said outputs, two of the said outputs having a equal weight, said third and fourth carry save adders each receiving at least one output from each of said first and second carry save adders and the first and second carry save adders being arranged to receive at least some of said inputs;

wherein the carry save adder circuit is a 9 to 4 carry save adder circuit; and

wherein the first carry save adder is a 5 to 3 carry save adder and the second, third and fourth carry save adders are 3 to 2 carry save adders.

2. (Original) A carry save adder circuit as claimed in claim 1, wherein at least one of said inputs is input to at least one of said third and fourth carry save adders.

3-4. (Canceled)

5. (Currently Amended) A carry save adder circuit as claimed in claim [[3]] 1, wherein the first to fifth inputs are input to the first carry save adder and the sixth to eighth inputs are provided to the second carry save adder.

6. (Original) A carry save adder circuit as claimed in claim 5, wherein the ninth input is input directly to one of the third and fourth carry save adders.

7. (Canceled)

8. (Currently Amended) ~~A carry save adder circuit as claimed in claim 7,~~ A carry save adder circuit for reducing the number of inputs to a lower number of outputs, said carry save adder circuit comprising four carry save adders, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a second of said layers, said third and fourth carry save adders being arranged to provide said outputs, two of the said outputs having a equal weight, said third and fourth carry save adders each receiving at least one output from each of said first and second carry save adders and the first and second carry save adders being arranged to receive at least some of said inputs;

wherein the carry save adder circuit is a 7 to 4 carry save adder circuit; and

wherein the first and third carry save adders are 3 to 2 carry save adders and the fourth carry save adder is a half adder.

9. (Currently Amended) A carry save adder circuit as claimed in claim [[7]] 8, wherein the first and third inputs are input to the first carry save adder and the fourth to sixth inputs are provided to the second carry save adder.

10. (Original) A carry save adder circuit as claimed in claim 9, wherein the seventh input is input directly to one of the third and fourth carry save adders.

11. (Currently Amended) A carry save adder circuit for reducing nine inputs for four outputs, said carry save adder circuit comprising four carry save adders, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a second of said layers, said third and fourth carry save adders being arranged to provide said outputs, two of the said outputs having a equal weight, said third and fourth carry save adders each receiving at least

one output from each of said first and second carry save adders and the first and second carry save adders being arranged to receive at least some of said inputs, the first carry save adder being a 5 to 3 carry save adder and the second, third and fourth carry save adders being 3 to 2 carry save adders.

12. (Original) A carry save adder circuit as claimed in claim 11, wherein the first carry save adder receives five inputs, the second carry save adder receives three inputs, one of the third and fourth carry save adders receives an input and the sum output of the first and second carry save adders, the carry outputs of the first and second carry save adders being connected to the other of the third and fourth carry save adders.

13. (Currently Amended) A carry save adder circuit for reducing seven inputs to four outputs, said carry save adder circuit comprising four carry save adder units, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a second of said layers, said third and fourth carry save adders being arranged to provide said outputs, two of the said outputs having an equal weight, said third and fourth carry save adders each receiving at least one output from each of said first and second carry save adders and the first and second carry save adders being arranged to receive at least some of said inputs, the first, second and third carry save units being 3 to 2 carry save adders and the fourth carry save adder being a half adder.

14. (Previously Presented) A carry save adder circuit as claimed in claim 13, wherein the first and second carry save adders each receive three inputs, one of the third and fourth carry save adders receiving an input and the sum outputs of the first and second carry save adders, the carry output of the first and second carry save adders being connected to the other of the third and fourth carry save adders.

15. (Original) A carry save adder circuit as claimed in claim 1, wherein four outputs are provided, one of the outputs having a weight of 2^i , two of the outputs having a weight of 2^{i+1} , and one of the outputs having a weight of 2^{i+2} .

16. (Canceled)

17. (Currently Amended) A unit as claimed in claim ~~[[16]]~~ 21, wherein there is no carry output provided from the output of the first layer of each carry save adder to an adjacent carry save adder.

18. (Currently Amended) An arithmetic unit as claimed in claim ~~[[16]]~~ 21, wherein no signal is received by the second layer of each carry save adder from an adjacent carry save adder.

19. (Currently Amended) A unit as claimed in claim ~~[[16]]~~ 21, wherein the number of bits from the respective partial products is the same or less than the number of inputs to the respective carry save adder circuit processing said respective bits.

20. (Original) A unit as claimed in claim 1, wherein there is no data propagation between the third and fourth carry save adders.

21. (Previously Presented) An arithmetic unit for processing a plurality of partial products, said unit comprising a plurality of carry save adder circuits, each said carry save adder circuit being arranged to reduce nine inputs to four outputs, said carry save adder circuit comprising four carry save adders, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a second of said layers said third and fourth carry save adders each receiving at least one output from each of said first and second carry save adders, the first carry save adder being a 5 to 3 carry save adder and the second, third and fourth carry save

adders being 3 to 2 carry save adders, wherein the inputs to each of said carry save adder circuits are provided by said plurality of partial products.

22. (Previously Presented) An arithmetic unit for processing a plurality of partial products, said unit comprising a plurality of carry save adder circuits each said carry save adder circuit, being arranged to reduce seven inputs to four outputs, said carry save adder circuit comprising four carry save adder units, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a second of said layers said third and fourth carry save adders each receiving at least one output from each of said first and second carry save adders, the first, second and third carry save units being 3 to 2 carry save adders and the fourth carry save adder being a half adder, wherein the inputs to each of said carry save adder circuits are provided by said plurality of partial products.

23. (Canceled)

24. (New) A unit as claimed in claim 22, wherein there is no carry output provided from the output of the first layer of each carry save adder to an adjacent carry save adder.

25. (New) An arithmetic unit as claimed in claim 22, wherein no signal is received by the second layer of each carry save adder from an adjacent carry save adder.

26. (New) A unit as claimed in claim 22, wherein the number of bits from the respective partial products is the same or less than the number of inputs to the respective carry save adder circuit processing said respective bits.